WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a workpiece;

a first transistor formed in a first region of the workpiece, the first transistor having a first source, a first drain, and a first gate;

a second transistor formed in a second region of the workpiece, the second transistor having a second source, a second drain, and a second gate;

a first insulating layer disposed over at least the second source or the second drain of the second transistor; and

a second insulating layer disposed over at least the first source or the first drain of the first transistor and over the first insulating layer over the second source or the second drain of the second transistor, the second insulating layer comprising a different material than the first insulating layer.

2. The semiconductor device according to Claim 1, wherein the second insulating layer increases surface tension of a top surface of the first source or the first drain of the first transistor, and wherein the first insulating layer comprises a material that reduces surface tension of a top surface of the second source or the second drain of the second transistor.

3. The semiconductor device according to Claim 2, wherein the first transistor comprises a first channel region disposed beneath the first gate, wherein the second transistor comprises a second channel region disposed beneath the second gate, wherein the second insulating layer increases surface tension in the first channel region of the first transistor, and wherein the first insulating layer reduces surface tension in the second channel region of the second transistor.

4. The semiconductor device according to Claim 1, wherein the first insulating layer comprises an oxide material and the second insulating layer comprises a nitride material or a carbon-containing material.

5. The semiconductor device according to Claim 4, wherein the first insulating layer comprises silicon dioxide or silicon oxynitride, and the second insulating layer comprises silicon nitride or silicon-carbon.

6. The semiconductor device according to Claim 4, wherein the first insulating layer comprises a thickness of about 400 Å or less, and wherein the second insulating layer comprises a thickness of about 850 Å or less.

7. The semiconductor device according to Claim 1, further comprising:

an interlevel dielectric (ILD) layer disposed over the first transistor and the second transistor;

a first contact formed within the ILD layer, the first contact making electrical contact to the first source or the first drain of the first transistor; and

a second contact formed within the ILD layer, the second contact making electrical contact to the second source or the second drain of the second transistor.

8. The semiconductor device according to Claim 7, wherein the ILD layer comprises a material etchable selective to the material of the second insulating layer.

9. The semiconductor device according to Claim 7, wherein the ILD layer comprises an oxide material, and wherein the second insulating layer comprises a nitride material or carbon-containing material.

10. The semiconductor device according to Claim 7, further comprising a first bond pad disposed over the first contact, and a second bond pad disposed over the second contact.

11. The semiconductor device according to Claim 1, wherein the first region of the workpiece is proximate the second region of the workpiece, wherein the semiconductor device comprises a complimentary metal oxide semiconductor (CMOS) device, wherein the first transistor comprises an n channel metal oxide semiconductor transistor (NMOS) device, and wherein the second transistor comprises a p channel metal oxide semiconductor transistor (PMOS) device.

12. The semiconductor device according to Claim 11, wherein the first source and the first drain of the first transistor are N+ doped, and wherein the second source and the second drain of the second transistor are P+ doped.

13. The semiconductor device according to Claim 1, further comprising a silicide layer disposed over the first source, the first drain, and the first gate of the first transistor, and over the second source, the second drain, and the second gate of the second transistor.

14. A complimentary metal oxide semiconductor (CMOS) device, the CMOS device comprising:

a workpiece;

a first transistor formed in a first region of the workpiece, the first transistor comprising an n channel metal oxide semiconductor transistor (NMOS) device, the first transistor having a first source, a first drain, and a first gate;

a second transistor formed in a second region of the workpiece, the second transistor comprising a p channel metal oxide semiconductor transistor (PMOS) device, the second transistor having a second source, a second drain, and a second gate;

a surface tension-reducing layer disposed over at least the first source or the first drain of the first transistor;

a surface tension-inducing layer disposed over at least the first source or the first drain of the first transistor and over the surface tension-reducing layer over the second source or the second drain of the second transistor, the surface tension-inducing layer comprising a different material than the surface tension-reducing layer;

an interlevel dielectric (ILD) layer disposed over the first transistor and the second transistor;

a first contact formed within the ILD layer, the first contact making electrical contact to the first source or the first drain of the first transistor; and

a second contact formed within the ILD layer, the second contact making electrical contact to the second source or the second drain of the second transistor.

15. The semiconductor device according to Claim 14, wherein the surface tension-inducing layer increases surface tension of a top surface of the first source or the first drain of the first transistor, and wherein the surface tension-reducing layer comprises a material that reduces surface tension of a top surface of the second source or the second drain of the second transistor.

16. The semiconductor device according to Claim 15, wherein the first transistor comprises a first channel region disposed beneath the first gate, wherein the second transistor comprises a second channel region disposed beneath the second gate, wherein the surface tension-inducing layer increases surface tension in the first channel region of the first transistor, and wherein the surface tension-reducing layer reduces surface tension in the second channel region of the second transistor.

17. The semiconductor device according to Claim 14, wherein the surface tension-reducing layer comprises an oxide material and the surface tension-inducing layer comprises a nitride material or a carbon-containing material.

18. The semiconductor device according to Claim 17, wherein the surface tension-reducing layer comprises silicon dioxide or silicon oxynitride, and the surface tension-inducing layer comprises silicon nitride or silicon-carbon.

19. The semiconductor device according to Claim 14, wherein the surface tension-reducing layer comprises a thickness of about 50 Å to about 300 Å, and wherein the surface tension-inducing layer comprises a thickness of about 200 Å to about 700 Å.

20. The semiconductor device according to Claim 14, wherein the ILD layer comprises a material that is etchable selective to the material of the surface tension-inducing layer.

21. The semiconductor device according to Claim 20, wherein the ILD layer comprises an oxide material, and wherein the surface tension-inducing layer comprises a nitride material or a carbon-containing material.

22. The semiconductor device according to Claim 14, wherein the first source and the first drain of the first transistor are N+ doped, and wherein the second source and the second drain of the second transistor are P+ doped.

23. The semiconductor device according to Claim 14, further comprising a silicide layer disposed over the first source, the first drain, and the first gate of the first transistor, and disposed over the second source, the second drain, and the second gate of the second transistor.

24. The semiconductor device according to Claim 14, further comprising a first bond pad disposed over the first contact, and a second bond pad disposed over the second contact.

25. A method of manufacturing a semiconductor device, the method comprising:

providing a workpiece;

forming a first transistor in a first region of the workpiece, the first transistor having a first source, a first drain, and a first gate;

forming a second transistor in a second region of the workpiece, the second transistor having a second source, a second drain, and a second gate;

forming a first insulating layer over at least the second source or the second drain of the second transistor; and

forming a second insulating layer over at least the first source or the first drain of the first transistor and over the first insulating layer over the second source or the second drain of the second transistor, wherein forming the second insulating layer comprises forming a different material than the first insulating layer.

26. The method according to Claim 25, wherein forming the first insulating layer over at least the second source or the second drain of the second transistor comprises:

forming the first insulating layer over the first source or the first drain of the first transistor and over the second source or the second drain of the second transistor; and

removing the first insulating layer from over the first source or the first drain of the first transistor.

27. The method according to Claim 26, wherein removing the first insulating layer from over the first source or the first drain of the first transistor comprises:

depositing a photoresist over the first insulating layer;

patterning the photoresist;

removing portions of the photoresist to expose portions of the first insulating layer; and

removing the exposed portions of the first insulating layer, using the photoresist as a mask.

28. The method according to Claim 25, wherein forming the second insulating layer comprises forming a material that increases surface tension of a top surface of the first source or the first drain of the first transistor, and wherein forming the first insulating layer comprises forming a material that reduces surface tension over the second source or the second drain of the second transistor.

29. The method according to Claim 28, wherein the first transistor comprises a first channel region disposed beneath the first gate, wherein the second transistor comprises a second channel region disposed beneath the second gate, wherein the second insulating layer increases surface tension in the first channel region of the first transistor, and wherein the first insulating layer reduces surface tension in the second channel region of the second transistor.

30. The method according to Claim 25, wherein forming the first insulating layer comprises forming an oxide material, and wherein forming the second insulating layer comprises forming a nitride material or a carbon-containing material.

31. The method according to Claim 30, wherein forming the first insulating layer comprises forming silicon dioxide or silicon oxynitride, and wherein forming the second insulating layer comprises forming silicon nitride or silicon-carbon.

32. The method according to Claim 25, wherein forming the first insulating layer comprises forming a material layer comprising a thickness of about 400 Å or less, and wherein forming the second insulating layer comprises forming a material layer comprising a thickness of about 850 Å or less.

33. The method according to Claim 25, further comprising:

forming an interlevel dielectric (ILD) layer over the first transistor and the second transistor;

forming a first contact within the ILD layer, the first contact making electrical contact to the first source or the first drain of the first transistor; and

forming a second contact within the ILD layer, the second contact making electrical contact to the second source or the second drain of the second transistor.

34. The method according to Claim 33, wherein forming the ILD layer comprises forming a material that is etchable selective to the material of the second insulating layer.

35. The method according to Claim 33, wherein forming the first contact comprises using the first insulating layer and the second insulating layer as an etch stop, and wherein forming the second contact comprises using the second insulating layer as an etch stop.

36. The method according to Claim 33, wherein forming the ILD layer comprises forming an oxide material, and wherein forming the second insulating layer comprises forming a nitride material or a carbon-containing material.

37. The method according to Claim 33, wherein forming the first contact and forming the second contact in the ILD layer comprise:

depositing a photoresist over the ILD layer;

patterning the photoresist with a pattern for the first contact and the second contact;

removing portions of the photoresist to expose portions of the ILD layer;

removing the exposed portions of the ILD layer using the photoresist as a mask, forming a first trench for the first contact and forming a second trench for the second contact; and

depositing a conductive material over the ILD layer to fill the first trench and the second trench, forming the first contact and the second contact, respectively, in the ILD layer.

38. The method according to Claim 25, wherein the first region of the workpiece is proximate the second region of the workpiece, wherein the semiconductor device comprises a complimentary metal oxide semiconductor (CMOS) device, wherein the first transistor comprises an n channel metal oxide semiconductor transistor (NMOS) device, the first source and the first drain of the first transistor being N+ doped, and wherein the second transistor comprises a p channel metal oxide semiconductor transistor (PMOS) device, the second source and the second drain of the second transistor being P+ doped.

39. The method according to Claim 25, further comprising forming a silicide over the first source, the first drain, and the first gate of the first transistor, and over the second source, the second drain, and the second gate of the second transistor.